Laurence E. LaForge, PhD, President and CEO. Previously professor with Embry-Riddle Aeronautical University. Three-time NASA Fellow, twice at the Jet Propulsion Laboratory; contributor, Deep Space 1. Principal Engineer, Digital Equipment Corporation, now part of Hewlett Packard; contributor to the VAX/VMS 8600, and to CHAS, a pioneering CAD/CAM suite for integrating VLSI design domains. More than 40 publications, including articles in the IEEE Transactions on Computers, the IEEE Transactions on Reliability, and the IEEE Transactions on Parallel and Distributed Processing. Baccalaureate: Massachusetts Institute of Technology. PhD: McGill University. Member, Institute for Electrical and Electronics Engineers.

Imagine the bar code applications we will craft for you! For example, our own RightCardWare software family bolsters person-to-person convenience. RightCardWare creates a high-density bar code containing name, telephone number, and more. This contact information can be typed, imported from programs like Microsoft Outlook, or read in from .VCF vCard files you may have seen attached to emails. RightCardWare prints these bar codes onto the backs of business cards. Client: Symbol Technologies.

Using our RightCardReader software, scan bar-coded business cards into Outlook, CardScan, or other personal information manager. Similar to Acrobat Reader, RightCardReader is free of charge. Error-free, and at the touch of a button, the RightCardWare family integrates standard papers, inks, printers, and scanners. Imagine the bar code applications we will craft for you!

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Deep Space 1, first probe propelled by an ion engine. Right Stuff of Tahoe professionals contributed to the avionics, power, and software subsystems
Imagine the modeling and test software we will craft for you! As shown below, for example, our own Connection Foundry family of software analyzes and synthesizes connectivity, using adaptive radio-frequency (RF) algorithms for conserving power in mobile ad hoc networks (MANETs). Client: Department of Homeland Security.

Screen shot above: one frame in a sequence illustrating RF channels whose power gains or shrinks, or which connect and disconnect, in response to the motions of nodes. Nodes represent software defined radios. Red and black: point-to-point RF channels correspond to the Delaunay triangulation, as it is known in the field of computational geometry. In blue: Dirichlet cells comprise the Voronoi diagram, mathematical dual of the Delaunay triangulation. Below: physical layer model, 16-node MANET, constant channel bit rate, constrained signal-to-interference-or-noise. Client: Department of Defense. Imagine the modeling and test software we will craft for you!

\[ W_r = \frac{G_r G_t}{(4\pi d/\lambda)^2} \]

Receive, transmit gain: \( G_r, G_t \)
Receive, transmit power: \( W_r, W_t \)
\( d/\lambda \): separation, in wavelengths

Since integrated circuit area is a prime determinant of both cost and yield, you should quantify the amount of redundancy to build: neither too little nor too much. Since signal delay increases as the square of wire length, you should know how to minimize the length of the longest wire. The Right Stuff of Tahoe is one of a very few firms that can optimize redundancy and wirelength, and then transform the attendant formulas into practical designs that achieve your objectives for dependability. Imagine the scientifically sound systems we will craft for you!

\[ \left(\frac{1}{at} + \frac{1}{t} \right) \ln \left[ \frac{1}{1-p} \right] - 1 \quad \text{and} \quad \frac{at}{(1-p)^2} = at \]

Maximum wirelength between \( t^{-1}[-\ln(1-p)]^2 \) and \( (1-p)^2 \)

L. E. LaForge. What designers of microelectronic systems should know about arrays spared by rows and columns. IEEE Transactions on Reliability. 39 (3), Sep-2000. 251-272

**Architectural Behavior**

Configuration rules, scale parameter \( t \):
1. Any \( at \) of \((a+c)\) columns may be selected from the \( t \times ct \) nominal array and \( ct \) spare columns.
2. Any \( t \) of \((1+b)t \) rows may be selected from the \( t \times ct \) nominal array and \( bt \) spare columns.
3. The columns of the spare rows may be connected, using at disjoint paths, to the columns selected by rule 1.

**Classical Fault Tolerant Array: Rows and Columns Dedicated as Spares**

**Architectural Floorplan**

**Transistor Level Layout**

**Chip Fabricated and Bonded**

**Count on The Right Stuff to Deliver Electronics and Avionics that Tolerate Defects Like These:**

- SRAM metal-to-metal short circuit
- DRAM transistor gate oxide pinhole

Wonder if you can do better than dedicated sparing? You bet you can! Much better, in fact. Contact us!

**The Right Stuff solves problems. Let us solve yours.**